

## **ABSTRACT OF THE DISCLOSURE**

A memory array configuration is provided that includes a plurality of magnetic cell junctions and a conductive line comprising a gate of a first transistor configured to  
5 enable a read operation for one of a plurality of magnetic cell junctions and a gate of a second transistor configured to enable a write operation for another of the plurality of magnetic cell junctions. Another memory array configuration is provided which includes a set of conductive structures serially coupled to a bit line spaced apart from and, in some embodiments, directly above a magnetic cell junction, a transistor coupled to the set of  
10 conductive structures and a program line collectively configured with the bit line to induce current flow through the set of conductive structures upon an application of a voltage to a gate of the transistor. A method for operating such a magnetic memory array is also contemplated herein.